



## **Generalized Emulation of Microcircuits**

The Generalized Emulation of Microcircuit technology was developed by the Sarnoff Corporation (Sarnoff) for the Defense Logistics Agency (DLA) and the Defense Supply Center Columbus (DSCC) to provide a solution to the diminishing manufacturing sources problem. The program was initiated by DLA in 1987 as a research and development project and transitioned into a production on-demand element in 1991. DSCC received program management responsibilities in 1997



and manages the program today. Utilizing a set of gate arrays and a single processing technology Sarnoff provides a continuing source of Form, Fit and Function replacements for non-procurable microcircuits. The microcircuits are supplied to the existing system documentation (source control drawings, standard military drawing, military slash sheets and/or other custom specifications) and the requirement for system documentation changes are minimized if not eliminated. GEM technology provides a continuing source of microcircuits originally produced with RTL, DTL, TTL, Schottky, ECL, NMOS, and CMOS technologies.

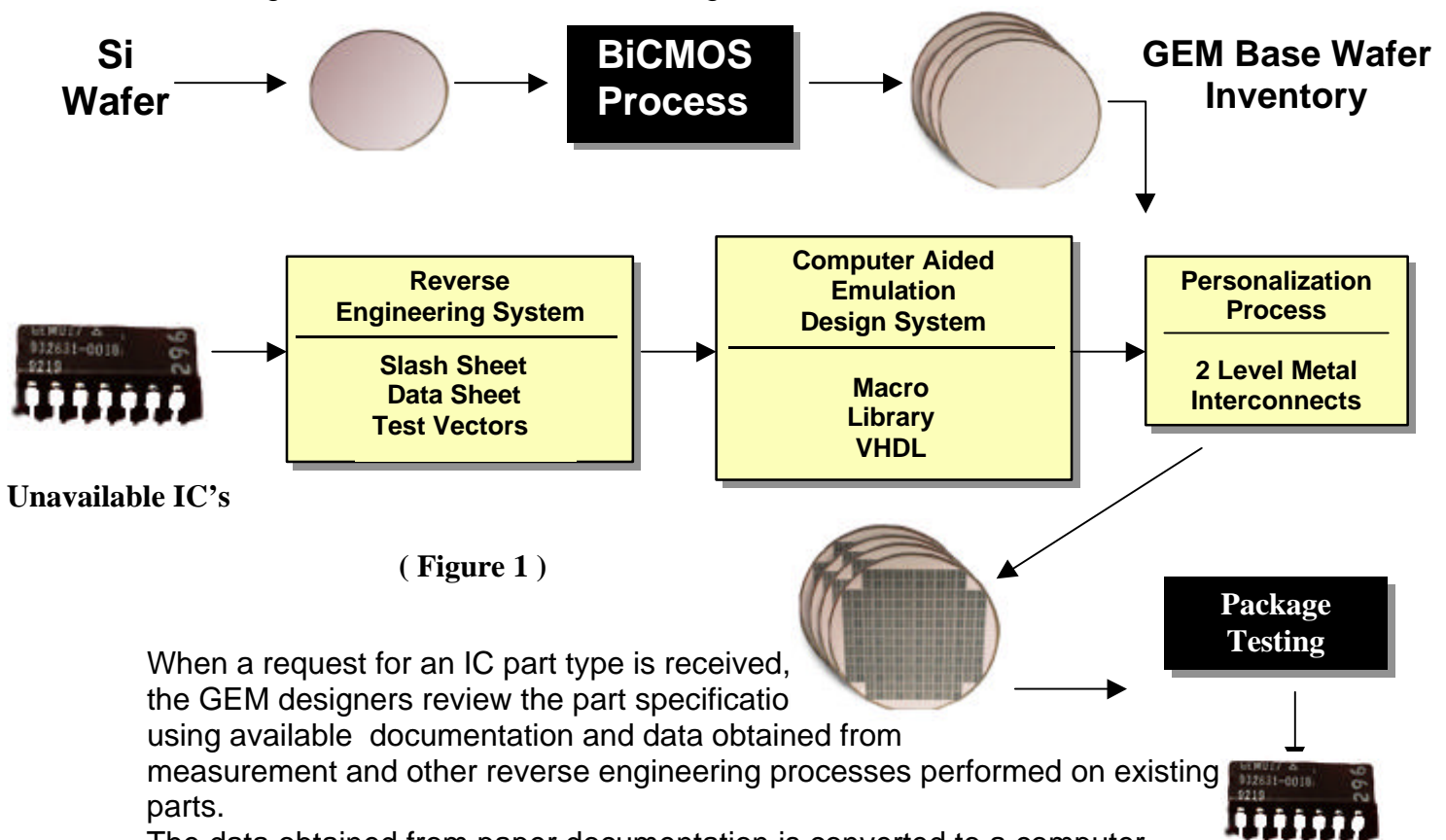
### **Applications**

The GEM approach has been successfully demonstrated by the fabrication of microcircuits which have been inserted and validated in several military systems. GEM microcircuits have passed engineering insertion tests in Army, Navy, and Air Force systems. For example, GEM parts were successfully applied to modules in the AN/SQS-56, AN/BQQ-5 and the AN/UYK-44 by the DDS program at NWSCC. CECOM, Fort Monmouth has made successful insertions of CMOS GEM microcircuits in the SINCGARS and AN/PRC70 radios. Warner Robins ALC is in the fifth year of a multi-year support program for the F-15. Fifty microcircuit types have been delivered for flight test and over 25 part types are in various stages of development.

These microcircuits were fabricated using the GEM BiCMOS technology. Examples include bipolar and MOS microcircuit technology families stretching chronologically from RTL to CMOS and from single function complexities to small microprocessors. These GEM microcircuits have a complete tracking history and meet all of the specifications of the original devices, including physical (package type, pin out), electrical (functional DC, dynamic, power) and environmental (ESD, temperature, hermeticity). GEM has redefined the way you obtain quality replacement microcircuits.

### Sarnoff's Ic Emulation Process

The GEM technology is based on families of 1.5µm and 3.5µm BiCMOS gate arrays which are personalized by a double-level metal process. The GEM BiCMOS gate array approach allows ICs which were originally manufactured in RTL, DTL, TTL, Schottky, CMOS and NMOS technologies to be produced from an inventory of GEM BiCMOS base wafers. The Sarnoff Production System for emulating microcircuits is illustrated in Figure 1.



( Figure 1 )

When a request for an IC part type is received, the GEM designers review the part specification using available documentation and data obtained from measurement and other reverse engineering processes performed on existing parts.

The data obtained from paper documentation is converted to a computer readable format and augmented by data obtained through electrical measurement

of existing sample parts. The result of the analysis is a GEM Design Specification that satisfies the original specification, and corrects any errors and ambiguities in the original documentation. In Sarnoff's experience, the part documentation obtained from data books, slash sheets, and OEM data are not always complete and must be verified. GEM designers complete the design, including simulation at the logic and device level, as required to verify that the part specification has been satisfied. One of the by-products of the emulation design is a VHDL (VHSIC Hardware Description Language) description of the

component. The completed circuit design is placed and routed using CAD software. Additional metalization is added as required to satisfy current density, bussing, and other requirements to provide the complete layout data in computer readable form for generation of the personalization mask set. The personalization mask may contain a mix of new and previously completed designs, as required to satisfy current orders.



### **Sarnoff's IC Emulation Process ( Cont... )**

The personalization masks are used to pattern the metal on the inventoried GEM base wafers to provide an implementation of a specific set of parts in one or more technologies supported by GEM. Personalized wafers are probed at Sarnoff to identify electrically good die. The probed die are sent to an external assembly vendor, audited for compliance with the QML requirements, to be diced and assembled. The die are assembled in the packages required for the specific orders. The packaged parts are either returned to Sarnoff for engineering evaluation, or sent to an external test vendor, audited for compliance with the QML requirements, for the screening and QCI tests required to satisfy the specific orders. Finished parts are returned to Sarnoff for shipping. GEM microcircuits satisfy all form, fit, and function specification requirements.

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